a plurality of word lines, each of which is arranged so as to intersect with both of said pair of data lines;

a plurality of dynamic memory cells, each of which is coupled to one of said word lines and to one of said data lines;

an amplifier having a pair of N-channel MOS transistors and a pair of P-channel MOS transistors, wherein each transistor of said pair of N-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of N-channel MOS transistors, wherein a drain of one of said pair of N-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of N-channel MOS transistors is coupled to the other of said pair of data lines, wherein each transistor of said pair of P-channel MOS transistor has a gate cross-coupled to a drain of the other transistor of said pair of P-channel MOS transistors, and wherein a drain of one of said pair of P-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of P-channel MOS transistors is coupled to the other of said pair of data lines, wherein said amplifier provides said data lines with a high-level potential and a low-level potential, respectively; and

a first switching MOS transistor having a source-drain path provided between said pair of data lines, wherein said first switching MOS transistor sets said pair of data

lines at an intermediate level between said high-level potential and said low-level potential when said plurality of memory cells are in a non-selected state.

2 1
~~21~~. A semiconductor memory according to claim ~~20~~, further comprising:

a second switching MOS transistor of N-channel type having a drain coupled to a source of each of said pair of N-channel MOS transistors and a source coupled to a first potential terminal; and

a third switching MOS transistor of P-channel type having a drain coupled to a source of each of said pair of P-channel MOS transistors and a source coupled to a second potential terminal.

cont A2

3 2
~~22~~. A semiconductor memory according to claim ~~21~~, wherein said first potential terminal has a potential level corresponding to said low-level potential, and

wherein said second potential terminal has a potential level corresponding to said high-level potential.

4 3
~~23~~. A semiconductor memory according to claim ~~22~~, wherein operation of said pair of N-channel MOS transistors is started at a time different from the time when operation of said pair of P-channel MOS transistors is started.

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